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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,034	10/31/2000	Joseph R. Zbiciak	TI-30553	8913

23494 7590 11/20/2003

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	7

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,034	ZBICIAK, JOSEPH R.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This communication is responsive to Amendment A, filed 10/1/2003.

2. Claims 1-15 are pending in this application. Claims 1 and 13 are independent claims. This action is made non-final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 7-8, and 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Baudendistel (U.S. 6,209,012).

Re claim 1, Baudendistel discloses in Figures 1 and 4 a method of performing a dot product operation (X and Y; col. 4 line 49) with rounding and shifting (22) in a microprocessor in response to a single rounding dot product instruction, the method comprising the steps of: fetching a first pair of elements (X including X_L and X_H) and a second pair of elements (Y including Y_L and Y_H); forming a first product of the first pair of elements (output of first multiplication as p0 = xh*yh in col. 4 line 29) and a second product of the second pair of elements (output of second multiplication as p1 = xl*yl in col. 4 line 29); combining the first product with the second product to form a combined

product (an adder in Figure 1 and col. 4 line 51); rounding the combined product to form an intermediate result (22 in Figure 1 and col. 5 lines 5-10); and shifting the intermediate result a selected amount to form a final result (22 in Figure 1 and col. 5 lines 5-10).

Re claim 2, Baudendistel discloses in Figures 1 and 4 further the step of shifting truncates a selected number of least significant bits of the intermediate result (claim 9 in col. 6 lines 6-7).

Re claim 3, Baudendistel further discloses in Figures 1 and 4 clearly in detail the step of rounding by adding a rounding value to the combined product (Figure 4 and col. 6 line 63) via an arithmetic circuit having a first input receiving first product (output of 20 of the first multiplication), a second input receiving second product (output of 20 of the second multiplication) and a carry input to a mid-position receiving rounding value (col. 5 lines 5-6) to form the intermediate result (Figure 4), and wherein the step of shifting shifts the intermediate result right by a selected shift amount (claim 9 in col. 6 lines 6-7).

Re claim 4, Baudendistel further discloses in Figures 1 and 4 the rounding value is 2^n and the selected shift amount is n+1 (col. 4 line 50 wherein the rounding occurs within 15 bits).

Re claim 5, Baudendistel further discloses in Figures 1 and 4 n has a fixed value of fifteen (col. 4 line 50 wherein the rounding occurs in 15 bits).

Re claim 7, Baudendistel further discloses in Figures 1 and 4 further disclose an overflow is not reported when an overflow occurs (col. 3 lines 25-27).

Re claim 8, Baudendistel further discloses in Figures 1 and 4 further disclose the step of fetching comprises the steps of: fetching a first operand (X); fetching a second

operand (Y); extracting one of the first pair of elements (xh) and one of the second pair of elements (xl) from the first operand; and extracting another one of the first pair of elements (yh) and another one of the second pair of elements (yl) from the second operand.

Re claim 10, Baudendistel further discloses in Figures 1 and 4 further disclose the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements (col. 5 lines 4-5).

Re claim 11, Baudendistel further discloses in Figures 1 and 4 further disclose the step of combining comprises adding the product of second pair of elements to the product of first pair of elements (col. 5 lines 7-8).

Re claim 12, Baudendistel further discloses in Figures 1 and 4 further disclose the steps of forming and combining operate on a plurality of pairs of elements (col. 4 lines 51).

Re claim 13, it is an apparatus claim of claim 1. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 14, it is an apparatus claim of claim 3. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 3.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Baudendistel (U.S. 6,209,012), as applied to claim 1 above, in view of Hsieh et al. (U.S. 5,995,122).

Re claim 6, Baudendistel discloses an overflow prevention, but does not implicitly disclose the step of rounding treats the intermediate result as a signed integer, such that when an overflow occurs, the intermediate will wrap from a largest positive value to a negative value. However, Hsieh et al. disclose in col. 10 lines 20-23 an instruction that would allow for saturation or wrap-around to handle overflow and underflow condition. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an instruction for wrap-around to handle overflow condition as seen in Hsieh et al.'s invention into Baudendistel's invention because it would enable to reduce the circuitry and efficiently handle an overflow condition.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being obvious over Baudendistel (U.S. 6,209,012) as applied to claim 1 above.

Re claim 9, Baudendistel further discloses in Figures 1 and 4 further disclose the step of forming treats both of the first and second pair of elements as signed number values (col. 3 lines 2-4). However, the examiner takes an official notice that the unsigned multiplication is less complex than the signed multiplication. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the second pair of elements as unsigned number for unsigned multiplication in

Baudendistel's invention because it would enable to reduce the circuitry and improve the system performance in general.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being obvious over Baudendistel (U.S. 6,209,012), as applied to claim 1 above, in view of Silberfenig (U.S. 6,243,594).

Re claim 15, Baudendistel does not disclose the above method being a cellular telephone as an integrated keyboard connected to the processor via a keyboard adapter; a display, connected to the processor via a display adapter; radio frequency (RF) circuitry connected to the processor; and an aerial connected to the RF circuitry. However, Silberfenig discloses in Figures 1-2 a cellular telephone as an integrated keyboard connected to the processor via a keyboard adapter; a display, connected to the processor via a display adapter; radio frequency (RF) circuitry connected to the processor; and an aerial connected to the RF circuitry. Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to use the above method in the device as disclosed in Silberfenig's invention because it would enable to improve the system of computing the dot products in signal processing (col. 19 lines 35-45).

Response to Arguments

9. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,854,758 to Kosuda et al. disclose a FFT computing unit and a FFT computation device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

November 6, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100